in accordance with 37 CFR § 1.121(c)(1)(ii). Any claim not accompanied by a marked-up version has not been changed relative to the immediate prior version, except that marked-up versions are not being supplied for any added claim or canceled claim.

CLAIMS

12. (Thrice Amended) A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface; and

unevenly removing material from the first uppermost surface of the conductive plug without using masking material over the first uppermost surface between the pair of conductive lines to define an uneven second uppermost surface at least a portion of which is disposed elevationally higher than the conductive lines and to reduce a width of the conductive plug from what it was prior to said unevenly removing.

13. The method of claim 12, wherein the unevenly removing material of the conductive plug comprises facet etching the conductive plug.

16. The method of claim 12, wherein the forming of the conductive plug comprises forming the uneven uppermost surface of the plug to have a central region and a corner region joined therewith, and the unevenly removing material comprises removing more material from the corner region than from the central region of the first uppermost surface.

4 21. (Twice Amended) A method of increasing alignment tolerances between bit line contact material and storage capacitors in a DRAM comprising beveling at least one corner of a conductive plug formed over a diffusion region with which a bit line is to electrically communicate effectively to reduce a width of the conductive plug, the beveling changing a first generally even uppermost surface of the conductive plug to a second generally uneven uppermost surface, the plug uppermost surface being outwardly exposed over the diffusion region during the beveling.

22. (Thrice Amended) A method of forming DRAM circuitry comprising: forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface over the node location having a generally uniform surface and having a width terminating over respective conductive lines of the pair of conductive lines; and

etching material of the conductive plug through the first uppermost surface to define a second uppermost surface which is generally non-planar and at least a portion of which is disposed elevationally higher than the conductive lines and to reduce the width of the conductive plug.

23. The method of claim 22, wherein the etching of the material of the conductive plug comprises facet etching the conductive plug.

47. The method of claim 21 comprising beveling at least two corners of the conductive plug.

Cancel claims 48-50.

53. (Amended) A method of increasing alignment tolerances between bit line contact material and storage capacitors in a DRAM comprising beveling at least one corner of a conductive plug formed over a diffusion region with which a bit line is to electrically communicate effectively to reduce a width of the conductive plug, the beveling changing a first generally even uppermost surface of the plug to a second generally uneven uppermost surface, wherein the beveling is effective to reduce a height of the conductive plug over the diffusion region.

956. (Amended) A semiconductor processing method of forming integrated circuitry comprising:

forming a pair of spaced and adjacent conductive contact projections over a substrate, the conductive contact projections having respective widths and a generally even first uppermost surface;

C6 etching at least one of the conductive contact projections effective to reduce its width, and form a generally uneven second uppermost surface;

forming insulative material over the conductive contact projections after the etching;

etching at least one contact opening through the insulative material to at least one of the conductive contact projections proximate the other of the conductive contact projections; and

wherein the one projection has an uppermost surface and the etching of the one projection etches material of the one projection from an entirety of the uppermost surface.

57. (Amended) A semiconductor processing method of forming integrated circuitry comprising:

forming a pair of spaced and adjacent conductive contact projections over a substrate, the conductive contact projections having respective widths and a generally even first uppermost surface;

etching at least one of the conductive contact projections effective to reduce its width, and form a generally uneven second uppermost surface;

forming insulative material over the conductive contact projections after the etching;

etching at least one contact opening through the insulative material to at least one of the conductive contact projections proximate the other of the conductive contact projections; and

wherein at least the one projection has an uppermost surface which is substantially planar immediately prior to the etching of the one projection.

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58. (Amended) A semiconductor processing method of forming integrated circuitry comprising:

forming a pair of spaced and adjacent conductive contact projections over a substrate, the conductive contact projections having respective widths and a generally even first uppermost surface;

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etching at least one of the conductive contact projections effective to reduce its width, and form a generally uneven second uppermost surface;

forming insulative material over the conductive contact projections after the etching;

etching at least one contact opening through the insulative material to at least one of the conductive contact projections proximate the other of the conductive contact projections; and

wherein the conductive projections have outermost surfaces which are entirely outwardly exposed during the etching of the at least one projection.

59. A method of forming DRAM circuitry comprising:

forming a pair of spaced-apart, insulated conductive lines over a substrate, the conductive lines defining a node location therebetween;

forming insulative material over the node location and between the conductive lines;

forming an opening through the insulative material and between the lines to proximate the node location;

forming conductive material within the opening over the node location, the conductive material comprising an outer portion received elevationally outward of the insulated conductive lines, the conductive material having side surfaces which project away from the node location and terminate proximate an upper surface, the side surfaces and upper surface defining at least one corner region, the side surfaces defining a maximum width of the outer portion of the conductive material within the opening; and

beveling the at least one corner region effective to reduce the maximum width of the outer portion of the conductive material above the conductive lines and etching at least some of the conductive material away from an entirety of the upper surface.

30. (New) A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface;

unevenly removing material from the first uppermost surface of the conductive plug to define an uneven second uppermost surface at least a portion of which is disposed elevationally higher than the conductive lines and to reduce a width of the conductive plug from what it was prior to said unevenly removing; and

wherein the unevenly removing comprises removing material of the conductive plug from an entirety of the uppermost surface.

81. (New) A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface;

unevenly removing material from the first uppermost surface of the conductive plug to define an uneven second uppermost surface at least a portion of which is disposed elevationally higher than the conductive lines and to reduce a width of the conductive plug from what it was prior to said unevenly removing; and

wherein the uppermost surface is substantially planar immediately prior to the unevenly removing.

62. (New) A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface having a generally uniform surface and having a width;

etching material of the conductive plug to define a second uppermost surface which is generally non-planar and at least a portion of which is disposed elevationally higher than the conductive lines and to reduce the width of the conductive plug; and

wherein the etching etches material of the conductive plug from an entirety of the uppermost surface.

63. (New) A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface having a generally uniform surface and having a width;

etching material of the conductive plug to define a second uppermost surface which is generally non-planar and at least a portion of which is disposed elevationally higher than the conductive lines and to reduce the width of the conductive plug; and

wherein the uppermost surface is substantially planar immediately prior to the etching.